ASHOK KUMAR

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Phone no – 7791073195, 8278637527

OBJECTIVE

I look forward to an experience that is both intellectually and professionally valuable. I hope to see myself grow as a professional, as an individual working in an innovative and competitive world. I wish to contribute to the organization with hard work, sincerity, patience and dedication.

EDUCATIONAL PROFILE

Year	Qualification	University / Board	Percentage/ CGPA
2020 (Pursuing)	Ph.D	I.I.T., Jodhpur	9.00
2019	M.Tech (ECE)	M.N.I.T., Jaipur	9.44
2014	B. Tech. (ECE)	M.N.I.T., Jaipur	8.46
2009	AISSC (Class XII)	C.B.S.E	77.20
2007	AISSE (Class X)	C.B.S.E	79.20

INDUSTRIAL EXPERIENCE

- **Intern at INTEL INDIA Technology Pvt. Ltd. Bangalore   4th July 2018 - 5th July 2019**
  Pre-Silicon Core Performance Back-end Team - Graduate Technical Intern
    - Working as Digital Design Engineer in Intel Core IP team as Circuit Design Engineer in Core team at Intel which is responsible for designing the core of the processors.
    - Responsible for designing and implementing modules from RTL specification.
    - The major project work at INTEL involves the design of lower technology nodes basically 14nm/10nm, implementation and optimization of functional unit blocks of microprocessor core and drive them to signoff with timing closure (STA), power reduction and Quality fixes.
- Completed Eight weeks of internship at the Defence Lab. Jodhpur (DRDO) in May-June, 2013

SOFT SKILLS

- Operating System   Windows (XP/Vista/7/8/10), Microsoft office
- Languages   C, Assembly, Verilog.
- Tools   EDEN (Intel specified) for Schematic and Layout Design. TANGO, DUET, and POET (Intel specified) for Timing, Quality and power.
                  H-Spice, Matlab, Linux (RHCE), Silvaco, TCAD, Opti System, Rsoft, CST Studio.

ACADEMIC PROJECTS SUMMARY

Tech. Summer Internship

Title   **Intercom using LM386 (intercommunication device).**
Description Developed a stand-alone voice communications system for use in Military tank, within a building or small collection of buildings.   Duration: -May'27 – July'12, 2013

M.Tech. Final Project

Title   **Timing and Power Optimization of Functional Unit Block in High Speed Core**
Tool   EDEN, SEQVER, TANGO, DUET and POET
Description The core is periodically advancing towards new challenges with a shrink in the transistor size. Transistor technology advancement has given a superior platform for fabricating high-

performance multi-core processors with several innovative features. With every new generation core designing there comes the requirement to meet certain targets. From a designer point of view , the new challenges in present day projects includes more stringent timing convergence and rigorous power reduction

M.Tech. Minor Project

Title | **Performance Analysis (2D and 3D Simulation) of Bottom Gate Thin Film Transistor**
Tool | Silvaco, TCAD
Description | A thin-film transistor (TFT) is a special kind of field-effect transistor made by depositing. Thin films of an active semiconductor layer as well as the dielectric layer and metallic contacts over a supporting (but non-conducting) substrate. The bottom gate thin-film transistor having zinc oxide as activating layer (channel), Silicon dioxide as the insulating layer on lightly doped p-type Silicon substrate and source, gate and drain are made of Al material.

B.Tech Project

Title | **Ground water level estimation and fabrication**
Description | The purpose of this project is to develop a low cost, easily repairable, indigenous, reliable ground water monitoring system. This model can measure the height and the temperature of ground water. In our approach, we implemented the water level detector with the help of two transistors. A local server was used to store the ground water level measurements, updated on an hourly basis.

ACHIEVEMENTS

- Participated in a one week Faculty Development Program on "5G Communication" jointly organized by the Deptt. of Electronics & Communication Eng. and the ICT Academy, M.N.I.T., Jaipur
- Won 2nd prize in the JUST A TOUCH (An event of electronics) in TAKASH"12 (A national level technical festival held at IIT, Jodhpur).
- Won 2nd prize in the DISCO LIGHT (An electronics event) in PRIMAVERA'12 (A national technical cum cultural fest held in MNIT, JAIPUR).
- Won 3rd prize in the PIEZO ALERT in NEURON-12 (A national technical fest held in MNIT, JAIPUR in which more than 120 teams participated)
- Worked as an EVENT HEAD of ROBOLYMPICS in NEURON-12
- Participated in the college level Texas Instruments Innovation Challenge-India Analog Design Contest 2014 conducted under Texas Instruments (India) University program.
- Participated in the Rover Research competition (A manually controlled Robot capable of transportation) in the INTER NIT Robotics Competition-2011 held in MANIT, Bhopal.
- Won 1st prize in the 11th National Youth Parliament of Vidyalaya at the Regional level (Organized by the Navodaya Vidyalaya Samiti)
- Qualified the GATE- 2016 qualified with a score of 383 and ranked 14812.
- Hold a NCC, "A" Certificate.
- An active member of SPIC MACAY & ELECTRONICA AND ITIKA Society, M.N.I.T., Jaipur. Worked as a Volunteer in NEURON' 10 (National Technical and Cultural Festival).

PERSONEL INFORMATION

Father's Name: MADA RAM

Mother's Name: ANCHI DEVI

Date of birth   :   01-05-1992

Sex   :   MALE

Marital Status: Single

Hobbies: Social Service; Playing Volleyball; Listening Music

DECLARATION

I hereby declare that the information furnished above is true to the best of my knowledge.

Ashok Kumar