

PALASH DAS

Assistant Professor, Department of CSE, IIT Jodhpur, Rajasthan, Pin-342030,

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EDUCATION

Doctor of Philosophy (Ph.D.) in Computer Science and Engineering (CSE). July 2015 - April 2022

Indian Institute of Technology Guwahati, Guwahati.

Thesis Title: Near-Memory acceleration of Convolutional Neural Networks by exploiting Parallelism, Sparsity, and Redundancy.

Supervisor: **Prof. Hemangee K. Kapoor**, Department of CSE, IIT Guwahati.

Master of Engineering (M.E.) in CSE.

July 2011 - July 2013

Indian Institute of Engineering Science and Technology, Shibpur.

Thesis Title: Designing and Synthesis of Reversible Circuits.

Supervisor: **Prof. Susanta Chakraborty**, Department of Computer Science and Technology, IEST Shibpur.

Bachelor of Technology (B.Tech.) in CSE.

August 2005 - August 2009

West Bengal University of Technology, India.

Higher Secondary Examination (H.S.), Class XII.

July 2003 - June 2005

Raiganj Coronation High School (W. B.C.H.S.E).

Madhyamik Examination, Class X.

July 2001 - June 2003

Raiganj Coronation High School (W.B.B.S.E).

RESEARCH INTEREST AND SKILLS

Research Area	Machine Learning Accelerators, Emerging Memory Technologies, Hardware Designing, Computer Architecture, Near-Memory Processing.
Programming Languages	Verilog, C, C++, CORE JAVA, JSP, JDBC, SWING.
Simulators	Vivado (HLS), Xilinx ISE, Gem5, Cadence, McPAT, CACTI.
Working Platforms	Windows, Linux.
Fundamentals	Computer Organizations and Architectures, Digital Electronics, Operating Systems, Data Structures and Algorithms, Principle of Programming language.

HONORS, AWARDS, AND FELLOWSHIPS

- Intel Fellow. September 2020 - August 2021
- NET [CBSE-UGC NET] Qualified for the post of Assistant Professor. June-2015
- GATE Qualified. March-2015
- MHRD Fellow. July 2015 - August 2020
- Certificate of Appreciation for Quality Teaching and Academic Performance (From Dumkal Institute of Engineering and Technology). September-2014
- National scholarships merit certificate holder for class X (From Govt. of West Bengal). June-2003
- Resource Person in the workshop under the strengthening component of DBT-STAR College Scheme, Ministry of Science and Technology, Govt. of India. January-2021
- Received ACM India-IARCS travel grant for DATE 2022 conference. March-2022
- Accepted travel grant for DAC 2022 conference. May-2022
- Received fellowship and student travel grant support for presenting a full paper in 31st International Conference on VLSI Design (VLSID). January-2018

WORK EXPERIENCE

Assistant Professor in the department of CSE.

August 2022 - till date

IIT Jodhpur, Rajasthan, India.

- Involved in research in the broad domain of Computer Architecture.
- Delivering lectures on several undergraduate (UG) / postgraduate (PG) courses.

Research Scholar and Teaching Assistant in the department of CSE.

July 2015 - April 2022

IIT Guwahati, Assam, India.

- Involved in full-time research in the broad domain of Computer Architecture.
- Worked as a Technical Assistant in the courses like Parallel Computer Architecture (CS527), Digital Design (CS221), Computer Organization and Architecture (CS222), Hardware Lab (CS223), and System Software.

Assistant Professor in the department of CSE.

August 2009 - July 2015

Dumkal Institute of Engineering and Technology approved by AICTE and Affiliated to MAKAUT.

- Delivered lectures on several undergraduate (UG) courses like Introduction to Programming, Object Oriented Technology and UML, Operating System, and Computer Organization and Architecture in the department of CSE.
- Supervised the final year UG projects.
- Received **Certificate of Appreciation for Quality Teaching and Academic Performance.**

RESEARCH PUBLICATION

International Journals: 6

1. Atul Kumar, Dipika Deb, Shirshendu Das, and **Palash Das**. “edAttack: Hardware Trojan Attack on On-Chip Packet Compression.” IEEE Design and Test journal, 2023 (Accepted through NOCS).
2. **Palash Das**, Shashank Sharma, and Hemangee K. Kapoor. “ALAMNI: Adaptive LookAside Memory based Near-Memory Inference Engine for Eliminating Multiplications in Real-Time.” IEEE Transactions on Computers (TC), 2022. **Impact Factor 3.131**
3. **Palash Das** and Hemangee K. Kapoor. “CLU: A near-memory accelerator exploiting the parallelism in Convolutional Neural Networks.” ACM Journal on Emerging Technologies in Computing Systems (JETC), Vol. 17, No.2, Pages 1-25, 2021. **Impact Factor 1.652**
4. **Palash Das** and Hemangee K. Kapoor. “nZESPA: A Near-3D-Memory Zero Skipping Parallel Accelerator for CNNs.” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Volume 40, Issue 8, Pages 1573 - 1585, 2020. **Impact Factor 2.807**
5. Bikromaditty Mondal, **Palash Das**, Pradyut Sarkar, and Susanta Chakraborty (2014), “A Comprehensive Fault Diagnosis Technique for Reversible Logic Circuit.” Computers and Electrical Engineering”, ELSEVIER, Vol 40.7, Pages 2259-2272, 2014. **Impact Factor 3.818**
6. **Palash Das**, Bikromaditty Mondal (2013), “Extended K-Map for Minimizing Multiple Output Logic Circuits.” International Journal of VLSI Design and Communication Systems (VLSICS), Vol. 4, No.4, Pages 1-8, August 2013. **Impact Factor 1.278**

International Conferences: 8

1. **Palash Das** and Hemangee K. Kapoor, “NDIE: A Near DRAM Inference Engine Exploiting DIMM’s Parallelism.” Asia Pacific Conference On Circuits And Systems (APCCAS), IEEE, 2023 (Accepted).
2. Atul Kumar, Dipika Deb, Shirshendu Das, and **Palash Das**, “edAttack: Hardware Trojan Attack on On-Chip Packet Compression.” International Symposium on Networks-on-Chip (NOCS) 2023, in association with IEEE Design and Test journal.
3. **Palash Das**, Ajay Joshi, and Hemangee Kapoor, “Hydra: A near hybrid memory accelerator for CNN inference.” Design, Automation and Test in Europe (DATE), pp. 1017-1022, 2022.

4. Imlijungla Longchar, **Palash Das**, and Hemangee K. Kapoor, “ZaLoBI: Zero avoiding Load Balanced Inference accelerator.” 30th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), IEEE, 2022.
5. Chirag Joshi, **Palash Das**, Ashwini Kulkarni, and Hemangee K. Kapoor, “Dimming Hybrid Caches to Assist in Temperature Control of Chip MultiProcessors.” The 30th ACM Great Lakes Symposium on VLSI (GLSVLSI), Pages 487-492, ACM, 2020.
6. **Palash Das** and Hemangee K. Kapoor, “Towards Near Data Processing of Compare Operations in 3D-stacked memory.” The 28th ACM Great Lakes Symposium on VLSI (GLSVLSI), Pages 243-248, ACM, 2018.
7. **Palash Das**, Shivam Lakhotia, Prabodh Shetty, and Hemangee K. Kapoor, “Towards Near Data Processing of Convolutional Neural Networks.” 31st International Conference on VLSI Design (VLSID), Pages 380-385, IEEE, 2018.
8. **Palash Das**, Bikromaditty Mondal (2014), “Signature Analysis for Synthesis of Reversible Circuits.” 18th IEEE International Symposium on VLSI Design (VDAT), Pages 1-2, 2014.

Others: 3

1. **Palash Das** and Hemangee K. Kapoor, “Near-Memory Architectures for CNNs while Exploiting Parallelism, Sparsity, and Redundancy,” Design Automation Conference (DAC), 2022 (Ph.D. Forum accepted).
2. **Palash Das** and Hemangee K. Kapoor, “Accelerating CNN Inference Near to the Memory by Exploiting Parallelism, Sparsity, and Redundancy,” Design, Automation and Test in Europe (DATE), 2022 (Ph.D. Forum accepted).
3. **Palash Das** and Hemangee K. Kapoor, “CLU: A Near-Memory Accelerator Exploiting the Parallelism in Convolutional Neural Networks,” 15th Academic Research and Careers for Students Symposium (ARCS 2021).

INTERNSHIP/TRAININGS

- C++ from IBM. June 2007 - August 2007
- CJEV3 (JAVA) From NIIT. May-2009

PROJECTS

- ALAMNI: Adaptive LookAside Memory based Near-data Inference engine for eliminating multiplications in real-time (**Agency: Intel under PhD Fellowship Program**).
- Design and Development of C to JAVA Compiler using LEX and YACC [only primitive operations].
- Reversible Circuit Simulator for fault Detection using JAVA and Files [Results Published in ELSEVIER].
- Software Project Management System using JSP, JAVABEAN, JDBC.
- Website Development of Dumkal Institute of Engineering and Technology [Senior Member of Website Development Committee].
- Payroll System using J2EE.
- Online Banking System using J2EE.
- Pseudo Random Clustering System using Swing.

PERSONAL DATA

Date of Birth: 03 April 1987.
Gender: Male.
Nationality: Indian.

PROFESSIONAL SERVICES AND MEMBERSHIPS

- Program Committee Member of "Data Science - Scalable Algorithms and Analytics" Track of International Conference on High Performance Computing, Data, and Analytics (HiPC), 2023.
- Reviewer of IEEE Transactions on Parallel and Distributed Systems (TPDS), December 2021.
- Institute of Electrical and Electronics Engineers (IEEE): Membership Number-94218186.
- Association for Computing Machinery (ACM): Membership Number-7218679.

REFERENCES

Name: **Dr. Hemangee K. Kapoor**,
Designation: Professor of CSE, Vice President ACM
India Council.
Contact:
Department of CSE, IIT Guwahati,
Guwahati (Assam), Pin. 781 039, India.
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Name: **Dr. Ajay Joshi**,
Designation: Professor of ECE.
Contact:
Department of ECE, Boston University, USA,
8 St. Mary's St Boston,
MA 02215, Room 334.
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Name: **Dr. Aryabartta Sahu**,
Designation: Associate Professor of CSE.
Contact:
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Indian Institute of Technology Guwahati,
Guwahati (Assam), Pin. 781 039, India.
Tel: +91-3612582370, Email: asahu@iitg.ac.in

Name: **Dr. Arnab Sarkar**,
Designation: Associate Professor of Advanced Tech-
nology Development Centre (ATDC).
Contact:
Department of ATDC, IIT Kharagpur, WB
Pin. 721302, India. Tel: +91-3222-2-81954, Email:
arnab@atdc.iitkgp.ac.in

DECLARATION

I hereby declare that all the details furnished above are true to the best of my knowledge and belief.