Amplifier Figure of Merit (FOM)

• The gain-bandwidth product is commonly used to benchmark amplifiers.
  – We wish to maximize both the gain and the bandwidth.
• Power consumption is also an important attribute.
  – We wish to minimize the power consumption.

\[
\frac{\text{Gain} \times \text{Bandwidth}}{\text{Power Consumption}} = \frac{\left( g_m R_C \right) \left( \frac{1}{R_C C_L} \right)}{I_C V_{CC}} = \frac{1}{V_I V_{CC} C_L}
\]

Operation at low \( T \), low \( V_{CC} \), and with small \( C_L \) \( \rightarrow \) superior FOM
Bode Plot

• The transfer function of a circuit can be written in the general form

\[
H(j\omega) = A_0 \left(\frac{1 + \frac{j\omega}{\omega_{z1}}}{1 + \frac{j\omega}{\omega_{z2}}}\right) \left(\frac{1 + \frac{j\omega}{\omega_{p1}}}{1 + \frac{j\omega}{\omega_{p2}}}\right) \ldots
\]

- \(A_0\) is the low-frequency gain
- \(\omega_{zj}\) are "zero" frequencies
- \(\omega_{pj}\) are "pole" frequencies

• Rules for generating a Bode magnitude vs. frequency plot:
  - As \(\omega\) passes each zero frequency, the slope of \(|H(j\omega)|\) increases by 20dB/dec.
  - As \(\omega\) passes each pole frequency, the slope of \(|H(j\omega)|\) decreases by 20dB/dec.

Bode Plot Example

• This circuit has only one pole at \(\omega_{p1}=1/(R_C C_L)\); the slope of \(|A_v|\) decreases from 0 to -20dB/dec at \(\omega_{p1}\).

- In general, if node \(j\) in the signal path has a small-signal resistance of \(R_j\) to ground and a capacitance \(C_j\) to ground, then it contributes a pole at frequency \((R_j C_j)^{-1}\).
**A_v Roll-Off due to C_L**

- The impedance of $C_L$ decreases at high frequencies, so that it shunts some of the output current to ground.

\[
\lambda = 0
\]

\[
A_v = -g_m \left( R_D \parallel \frac{1}{j \omega C_L} \right)
\]

\[
A_{1f} = -g_m \left( \frac{1}{j \omega C_L} \right)
\]

**Pole Identification Example 1**

\[
|\omega_{p1}| = \frac{1}{R_G C_{in}}
\]

\[
|\omega_{p2}| = \frac{1}{R_D C_L}
\]
Pole Identification Example 2

\[ \lambda = 0 \]

\[
|\omega_{p1}| = \frac{1}{\left( R_G \parallel \frac{1}{g_m}\right)C_{in}}
\]

\[ |\omega_{p2}| = \frac{1}{R_D C_L} \]

Pole Identification Example 3

\[ \omega_{p1} = \frac{1}{R_S C_{in}} \]

\[ \omega_{p2} = \frac{1}{R_C C_L} \]
High-Frequency BJT Model

• The BJT inherently has junction capacitances which affect its performance at high frequencies.

Collector junction: **depletion** capacitance, $C_{\mu}$

Emitter junction: **depletion** capacitance, $C_{je}$, and also **diffusion** capacitance, $C_{b}$.

$$C_{\pi} \equiv C_{b} + C_{je}$$

BJT High-Frequency Model (cont’d)

• In an integrated circuit, the BJTs are fabricated in the surface region of a Si wafer substrate; another junction exists between the collector and substrate, resulting in substrate junction capacitance, $C_{CS}$.
Example: BJT Capacitances

- The various junction capacitances within each BJT are explicitly shown in the circuit diagram on the right.

MOSFET Intrinsic Capacitances

The MOSFET has intrinsic capacitances which affect its performance at high frequencies:
1. gate oxide capacitance between the gate and channel,
2. overlap and fringing capacitances between the gate and the source/drain regions, and
3. source-bulk & drain-bulk junction capacitances ($C_{SB}$ & $C_{DB}$).
High-Frequency MOSFET Model

• The gate oxide capacitance can be decomposed into a capacitance between the gate and the source \((C_1)\) and a capacitance between the gate and the drain \((C_2)\).
  
  – In saturation, \(C_1 \cong \frac{2}{3} \times C_{\text{gate}}\), and \(C_2 \cong 0\).
  – \(C_1\) in parallel with the source overlap/fringing capacitance \(\rightarrow C_{GS}\)
  – \(C_2\) in parallel with the drain overlap/fringing capacitance \(\rightarrow C_{GD}\)

Example

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CS stage...with MOSFET capacitances explicitly shown Simplified circuit for high-frequency analysis

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\[
\begin{align*}
C_G & \quad C_D & \quad C_S & \quad C_D \quad C_S \\
M_1 & \quad V_{in} & \quad M_2 & \quad V_{DD} & \quad C_{G2} \quad C_{DB2} \\
M_2 & \quad V_{out} & \quad M_1 & \quad V_{in} & \quad C_{G1} \quad C_{DS1} \\
V_{DD} & \quad V_{DD} & \quad V_{out} & \quad V_{out} & \quad C_{G1} \quad C_{DS1} + C_{DB2} + C_{G2}
\end{align*}
\]
Transit Frequency, $f_T$

The “transit” or “cut-off” frequency, $f_T$, is a measure of the intrinsic speed of a transistor, and is defined as the frequency where the current gain falls to 1.

Conceptual set-up to measure $f_T$

\[
\begin{align*}
I_{out} &= g_m V_{in} \\
I_{in} &= \frac{V_{in}}{Z_{in}}
\end{align*}
\]

As $f$ increases, $Z_{in}$ decreases

\[
\Rightarrow V_{in} = Z_{in} \Rightarrow I_{out} = g_m Z_{in} = g_m \left( \frac{1}{j\omega_C C_{in}} \right) = 1
\]

\[
\Rightarrow \omega_C = \frac{g_m}{C_{in}}
\]

\[
I_{out} = \frac{g_m V_{in}}{C_{in}}
\]

\[
2\pi f_T = \frac{g_m}{C_{GS}}
\]
Dealing with a Floating Capacitance

- Recall that a pole is computed by finding the resistance and capacitance between a node and (AC) GROUND.
- It is not straightforward to compute the pole due to $C_{\mu 1}$ in the circuit below, because neither of its terminals is grounded.

![Circuit Diagram](image1)

Dealing with a Floating Capacitance

- Recall that a pole is computed by finding the resistance and capacitance between a node and (AC) GROUND.
- It is not straightforward to compute the pole due to $C_F$ in the circuit below, because neither of its terminals is grounded.

![Circuit Diagram](image2)
Miller’s Theorem

• If $A_v$ is the voltage gain from node 1 to 2, then a floating impedance $Z_F$ can be converted to two grounded impedances $Z_1$ and $Z_2$:

$$\frac{V_1 - V_2}{Z_F} = \frac{V_1}{Z_1} \Rightarrow Z_1 = Z_F \frac{V_1}{V_1 - V_2} = Z_F \frac{1}{1 - A_v}$$

$$\frac{V_1 - V_2}{Z_F} = -\frac{V_2}{Z_2} \Rightarrow Z_2 = -Z_F \frac{V_2}{V_1 - V_2} = Z_F \frac{1}{1 - 1/A_v}$$

Miller Multiplication

• Applying Miller’s theorem, we can convert a floating capacitance between the input and output nodes of an amplifier into two grounded capacitances.

• The capacitance at the input node is larger than the original floating capacitance.

$$Z_1 = \frac{Z_F}{1 - 1/A_v} = \frac{1/j\omega C_F}{1 - 1/A_v} = \frac{1}{j\omega (1 - 1/A_v) C_F}$$

$$Z_i = \frac{Z_F}{1 - A_v} = \frac{1/j\omega C_F}{1 - A_v} = \frac{1}{j\omega (1 - A_v) C_F}$$

$$C_F (1 - A_v)$$

$$C_F (1 - 1/A_v)$$
**Miller Multiplication**

- Applying Miller’s theorem, we can convert a floating capacitance between the input and output nodes of an amplifier into two grounded capacitances.
- The capacitance at the input node is larger than the original floating capacitance.

\[
A_0 \equiv -A_v
\]

\[
Z_1 = \frac{Z_F}{1 - A_v} = \frac{1}{j\omega C_F} \cdot \frac{1}{1 + \frac{1}{A_0}} \cdot \frac{1}{j\omega (1 + \frac{1}{A_0})C_F}
\]

**Application of Miller’s Theorem**

\[
\omega_{p,in} = \frac{1}{R_S (1 + g_m R_C) C_F}
\]

\[
\omega_{p,out} = \frac{1}{R_C \left(1 + \frac{1}{g_m R_C}\right) C_F}
\]

\[
W_{p,in} < W_{p,out}
\]

\[
\text{dominant pole determines bandwidth}
\]
Application of Miller’s Theorem

\[ \lambda = 0 \]

\[ \omega_{in} = \frac{1}{R_G(1 + g_m R_D) C_F} \]

\[ \omega_{out} = \frac{1}{R_D \left( 1 + \frac{1}{g_m R_D} \right) C_F} \]

Small-Signal Model for CE Stage
• Algebra of Sinusoidal and Bode Plots
• Ac analysis contd..